ADVANCED DIGITAL IC DESIGN (SESSION 12)
The white portions of the timeline bars in this illustration indicate that although early incarnations of these technologies may have been available, for one reason or another they weren’t enthusiastically received by the engineers working in the trenches during this period. For example, although Xilinx introduced the world’s first FPGA as early as 1984, design engineers didn’t really start using these little scamps with gusto and abandon until the early 1990s.
ASIC Design Styles

- **Full-Custom (every transistor hand-drawn)**
  - Best performance: as used by Intel uPs
- **Semi-Custom (Some custom + some cell-based design)**
  - Reduced design effort: AMD uPs plus recent Intel uPs
- **Cell-Based ASICs (Only use cells in standard library)**
- **Mask Programmed Gate Arrays**
  - Popular for medium-volume, moderate performance applications
- **Field Programmable Gate Arrays**
  - Popular for low-volume, low-moderate performance applications

- **Comparing styles:**
  - how much freedom to develop own circuits?
  - how many design-specific mask layers per ASIC?
World of Integrated Circuits

Integrated Circuits

- Full-Custom ASICs
- Semi-Custom ASICs
- User Programmable

- PLD
  - PAL
  - PLA
  - PML
- FPGA
  - LUT (Look-Up Table)
  - MUX
  - Gates
Two competing implementation approaches

**ASIC (Application Specific Integrated Circuit)**
- designs must be sent for expensive and time consuming fabrication in semiconductor foundry
- designed all the way from behavioral description to physical layout

**FPGA (Field Programmable Gate Array)**
- bought off the shelf and reconfigured by designers themselves
- no physical layout design; design ends with a **bitstream** used to configure a device
Which Way to Go?

**ASICs**
- High performance
- Low power
- Low cost in high volumes

**FPGAs**
- Off-the-shelf
- Low development cost
- Short time to market
- Re-configurability

High performance
Low power
Low cost in high volumes
Off-the-shelf
Low development cost
Short time to market
Re-configurability
What is an FPGA Chip?

- **Field Programmable Gate Array**
- A chip that can be configured by user to implement different digital hardware
- **Configurable Logic Blocks** and **Programmable Switch Matrices**
- **Bitstream to configure:** function of each block & the interconnection between logic blocks
Reconfigurable Logic

- **Logic blocks**
  - To implement combinational and sequential logic

- **Interconnect**
  - Wires to connect inputs and outputs to logic blocks

- **I/O blocks**
  - Special logic blocks at periphery of device for external connections

**Key questions:**

- How to make logic blocks programmable? (after chip has been fabbed!)
- What should the logic granularity be?
- How to make the wires programmable? (after chip has been fabbed!)
- Specialized wiring structures for local vs. long distance routes?
- How many wires per logic block?
Typical Components of an FPGA

- Logic Elements (LEs)
- Routing
- Input/Output logic
- Extra features
  - clocking
  - memory
  - memory interfaces
  - Multipliers
  - Etc.
A typical Logic Element

- Two main parts
  - Look-Up Table (LUT) for combinational logic
  - Flip Flop (FF) for sequential logic (memory)
Programmable Array Logic (PAL)

- Based on the fact that any combinational logic can be realized as a sum-of-products
- PALs feature an array of AND-OR gates with programmable interconnect
Anti Fuse Based Approach (Actel)

Rows of programmable logic building blocks + rows of interconnect

Anti-fuse Technology: Program Once

Use Anti-fuses to build up long wiring runs from short segments

8 input, single output combinational logic blocks
FFs constructed from discrete cross coupled gates
RAM Based Field Programmable Logic (Xilinx)
LUT Mapping

- N-LUT direct implementation of a truth table: any function of n-inputs.
- N-LUT requires $2^N$ storage elements (latches)
- N-inputs select one latch location (like a memory)

Why Latches and Not Registers?

4LUT example

Latches set by configuration bitstream
Configuring the CLB as a RAM

Memory is built using Latches not FFs

16x2

Read is same as a LUT Function!
FPGA (summary)

- FPGA provide a flexible platform for implementing digital computing
- A rich set of macros and I/Os supported (multipliers, block RAMS, ROMS, high-speed I/O)
- A wide range of applications from prototyping (to validate a design before ASIC mapping) to high-performance spatial computing
- Interconnects are a major bottleneck (physical design and locality are important considerations)
Facilities provided by modern FPGAs
## Summary of FPD programming technologies

<table>
<thead>
<tr>
<th>Switch type</th>
<th>Reprogrammable?</th>
<th>Volatile?</th>
<th>Technology</th>
</tr>
</thead>
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<tr>
<td>Fuse</td>
<td>No</td>
<td>No</td>
<td>Bipolar</td>
</tr>
<tr>
<td>EPROM</td>
<td>Yes (out of circuit)</td>
<td>No</td>
<td>UVCMOS</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Yes (in circuit)</td>
<td>No</td>
<td>EECMOS</td>
</tr>
<tr>
<td>SRAM</td>
<td>Yes (in circuit)</td>
<td>Yes</td>
<td>CMOS</td>
</tr>
<tr>
<td>Antifuse</td>
<td>No</td>
<td>No</td>
<td>CMOS+</td>
</tr>
</tbody>
</table>
How are FPGAs Used?

- Prototyping
  - Ensemble of gate arrays used to emulate a circuit to be manufactured
  - Get more/better/faster debugging done than with simulation

- Reconfigurable hardware
  - One hardware block used to implement more than one function

- Special-purpose computation engines
  - Hardware dedicated to solving one problem (or class of problems)
  - Accelerators attached to general-purpose computers (e.g., in a cell phone!)
Terminology

- **CPLD (complex PLD):** an arrangement of multiple SPLD-like blocks on a single chip. Alternative names are enhanced PLD (EPLD), superPAL, and megaPAL.

- **FPD (field-programmable device):** any integrated circuit used for implementing digital hardware that allows the end user to configure the chip to realize different designs. Programming such a device often involves placing the chip into a special programming unit, but some chips can also be configured “in system.” Another name for FPDs is programmable logic devices (PLDs); although PLDs are the same type of chips as FPDs, we prefer the term FPD because historically PLD denoted relatively simple devices.

- **FPGA (field-programmable gate array):** an FPD featuring a general structure that allows very high logic capacity. Whereas CPLDs feature logic resources with a wide number of inputs (AND planes), FPGAs offer narrower logic resources. FPGAs also offer a higher ratio of flip-flops to logic resources than do CPLDs.

- **HCPLD (high-capacity PLD):** term coined in trade literature refers to both CPLDs and FPGAs. We do not use this term here.

- **Interconnect:** the wiring resources in an FPD.

- **Logic block:** a relatively small circuit block replicated in an FPD array. A circuit implemented in an FPD is first decomposed into smaller sub-circuits that can each be mapped into a logic block. The term occurs mostly in the context of FPGAs but can also refer to a block of circuitry in a CPLD.
Terminology (continued)

- **Logic capacity**: the amount of digital logic that we can map into a single FPD, usually measured in units of the equivalent number of gates in a traditional gate array. In other words, we measure an FPD’s capacity as its comparable gate array size. Thus, we can refer to logic capacity as the number of two-input NAND gates.

- **Logic density**: the amount of logic per unit area in an FPD.

- **PAL (programmable array logic)**: a relatively small FPD containing a programmable AND plane followed by a fixed-OR plane.

- **PLA (programmable logic array)**: a relatively small FPD that contains two levels of programmable logic—an AND plane and an OR plane. (Although PLA structures are sometimes embedded into full-custom chips, we refer here only to user-programmable PLAs provided as separate integrated circuits.)

- **Programmable switch**: a user-programmable switch that can connect a logic element to an interconnect wire or one interconnect wire to another.

- **Speed performance**: the maximum operable speed of a circuit implemented in an FPD. For combinational circuits, it is set by the longest delay through any path, and for sequential circuits, it is the maximum clock frequency at which the circuit functions properly.

- **SPLD (simple PLD)**: usually a PLA or a PAL.