SESSION I: Operational Amplifiers

WAM 1.3: A Self-Compensated Monolithic Operational Amplifier with Low Input Current and High Slew Rate

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Monolithic operational amplifiers generally have acceptable performance in all respects except two: input current and current drift are often too high for applications involving high-source impedances, and maximum slew rates are too low to permit large signal operation beyond a few kHz. In this paper, circuit and device techniques which lead to significant improvements in both of these characteristics will be described.

Input current has been reduced by employing a special circuit configuration designed to operate with high betas (several thousand) and low-voltage transistors. These transistors are fabricated simultaneously with normal transistors by using modified diffusions to produce selectively both narrow and wide basewidths on the same wafer. At the same time, slew rates have been improved by reducing the ratio of first stage transconductance-to-operating current, \( g_m / I_1 \). It has been found that, for most well-designed amplifiers, reduction of \( g_m / I_1 \) is the only circuit modification (other than feedforward) available for speed improvement.

The basic amplifier configuration considered is essentially that of two cascaded voltage gain stages. Figure 1 shows a representative two-stage operational amplifier employing a single pole-splitting capacitor for phase compensation. As Figures 2 and 3 illustrate, the maximum slew rate for this amplifier is fixed, independent of operating current; i.e.,

\[
\frac{dV_o}{dt}_{\text{max}} = 2\omega_1 kT / q \tag{1}
\]

where \( \omega_1 \) is the frequency at which the open loop gain of the amplifier passes through unity. Typically, \( \omega_1 \) is set near the alpha cutoff frequency of the lateral PNP's used in the fabrication of the monolithic amplifier, since this provides maximum bandwidth without excessive phase buildup. Using \( \omega_1 \equiv \omega_{op} \) and noting that \( \omega_{op} / 2\pi \) is typically 3 MHz, the maximum slew rate given by equation (1) is \( \frac{dV_o}{dt}_{\text{max}} \approx 1 V / \mu s \). This limit can be shown to apply to most unity-gain stable monolithic operational amplifiers employing lateral PNP's and simple bipolar input stages, whether or not pole-splitting is used.

For a fixed \( \omega_1 \) the limit imposed in Figure 3 can be avoided only by decreasing the ratio of first stage transconductance-to-operating current. A simple way of doing this is to add resistance, \( R_e \), in series with each input transistor emitter. In this case, the maximum slew rate is found to be

\[
\frac{dV_o}{dt}_{\text{max}} = 2I_1 R_e \omega_1 (1 + r_{e1} / R_e) \tag{2}
\]

which increases directly with first stage operating current if

\[ I_1 > kT / q R_e \].

For the input stages, provisions are made to increase the effective values of both \( R_e \) and \( I_1 \).

A major problem which arises in the design of an integrated operational amplifier is the realization of a wideband monolithic equivalent to the PNP input stage: Figure 1. Figure 4 illustrates two differential lateral PNP-NPN composite connections which have a first transadmittance pole in the vicinity of \( \omega_{op} \). The operating current for these stages, \( I_1 \), is set in such a way that it is completely independent of the unpredictable beta of the lateral PNP's; Figure 4. Further, the collector-base voltage of the NPN transistors is held approximately to zero volts under all conditions, thus permitting the use of high beta, low-voltage input devices to reduce the amplifier input current.

Figure 5 shows the circuit for a monolithic operational amplifier incorporating the input stage of Figure 4a. This circuit exhibits a typical input current of 2 nA and an input offset current and current drift of 0.3 nA and 2 pA/C, respectively. The unity gain slew rate is 4 V/\( \mu s \) and the open loop voltage gain is 150,000. The input transistors operate with beta's of 4000, the effective first stage operating current, \( I_1 \), is 50 \( \mu \)A and the input transconductance, \( g_m = 1 / 2.5 \, k\Omega \). Other characteristics include internal capacitive compensation, input overvoltage and output short circuit protection. A photomicrograph of the die which incorporates all of the circuitry in Figure 5, including the 35 pF MOS compensation capacitor is shown in Figure 6.

A second version of the amplifier which has an effective \( I_1 \) of 0.5 mA, and \( g_m = 1 / 2.5 \, k\Omega \) has also been built. This amplifier has achieved a unity gain slew rate of 30 V/\( \mu s \), simultaneously with an input offset current of 40 nA, an open loop gain of 50,000 and a small signal bandwidth of 2.5 MHz.

The performance of these amplifiers rivals that of junction-FET input configurations in almost all respects. Input current and current drift are about the same in each, while voltage offset and drift are considerably better in the bipolar circuits.
FIGURE 2—Gain as a function of frequency for Figure 1 illustrating relationship between $C$ and $\omega_1$.

STEP RESPONSE:

\[
|A_v| \equiv \frac{1}{r_{e1}} \omega C
\]

\[
I = |A_v(\omega_1)| = \frac{1}{r_{e1} \omega_1 C}
\]

\[
C = \frac{1}{r_{e1} \omega_1}
\]

FIGURE 3—Calculation of slew rate ($dV_o/dt_{\text{max}}$) for the circuit in Figure 1 using $C$ from Figure 2.

\[
dV_o \bigg|_{\text{max}} = 2I_I r_{e1} \omega_1 = \frac{2kT}{q} \omega_1
\]

FOR BOTH (a) & (b) $I_I = (I_a - I_b)$

FIGURE 4—Lateral PNP-NPN differential amplifiers which have output operating currents independent of PNP $\beta$ and establish zero-volt collector-base potentials on the input transistors.

FIGURE 5—Complete schematic diagram for self-compensated low input current operational amplifier. Higher slew rates are obtained by operating with higher first stage currents.

FIGURE 6—Die photo for circuit in Figure 5. Dimensions are 56 mils x 63 mils.