Lecture 2
VLSI Testing Process and Equipment

- Motivation
- Types of Testing
- Test Specifications and Plan
- Test Programming
- Test Data Analysis
- Automatic Test Equipment
- Parametric Testing
- Summary
Motivation

- Need to understand some **Automatic Test Equipment (ATE)** technology
  - Influences what tests are possible
  - Serious analog measurement limitations at high digital frequency or in the analog domain
  - Need to understand capabilities for digital logic, memory, and analog test in **System-on-a-Chip (SOC)** technology

- Need to understand parametric testing
  - Used to take setup, hold time measurements
  - Use to compute $V_{IL}$, $V_{IH}$, $V_{OL}$, $V_{OH}$, $t_r$, $t_f$, $t_d$, $I_{OL}$, $I_{OH}$, $I_{IL}$, $I_{IH}$
Types of Testing

- **Verification testing**, characterization testing, or design debug
  - Verifies correctness of design and of test procedure – usually requires correction to design

- **Manufacturing testing**
  - Factory testing of all manufactured chips for parametric faults and for random defects

- **Acceptance testing** (*incoming inspection*)
  - User (customer) tests purchased parts to ensure quality
Testing Principle

INPUT PATTERNS
---11
---00
-----
-----
---01

DIGITAL CIRCUIT

OUTPUT RESPONSES
10---
00---
-----
---01---

STORED CORRECT RESPONSE

COMPARATOR

TEST RESULT
DEFINITION of TESTING

Device or Circuit under test

A KNOWN STIMULUS

DEVICE IN A KNOWN STATE

A KNOWN EXPECTED RESPONSE

EXAMPLE

IN_A
IN_B
IN_C
IN_D

Broadside Parallel Vector

with an unknown state

D Q
CLK

D Q
CLK

OUT_1
OUT_2

1 1
1 1
1 ^ 1
1 ^ 1

1 1
1 1
1 X 1
1 X 1

? ?

Figure 1-4 Definition of Testing
Analog Test (Traditional)

Analog device under test (DUT)

Stimulus

Response

Filter

DC

RMS

PEAK

ETC.
DSP-Based Mixed-Signal Test

Mixed-signal device under test (DUT)

Synthesizer
RAM D/A
Analog
Send memory
Digital

Digital signal processor (DSP)

Synchronization

Digitizer
A/D RAM
Analog
Receive memory
Digital

Vectors

Vectors
<table>
<thead>
<tr>
<th>Control</th>
<th>Data</th>
<th>Level of abstraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic values</td>
<td>Words</td>
<td>Logic level</td>
</tr>
<tr>
<td>(or sequences of logic values)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic values</td>
<td>Words</td>
<td>Register level</td>
</tr>
<tr>
<td>Instructions</td>
<td>Words</td>
<td>Instruction set level</td>
</tr>
<tr>
<td>Programs</td>
<td>Data structures</td>
<td>Processor level</td>
</tr>
<tr>
<td>Messages</td>
<td></td>
<td>System level</td>
</tr>
</tbody>
</table>

Levels of abstraction in information processing by a digital system
## Type of Testing

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Attribute of testing method</th>
<th>Terminology</th>
</tr>
</thead>
<tbody>
<tr>
<td>When is testing performed?</td>
<td>• Concurrently with the normal system operation</td>
<td>On-line testing</td>
</tr>
<tr>
<td></td>
<td>• As a separate activity</td>
<td>Concurrent testing</td>
</tr>
<tr>
<td>Where is the source of the stimuli?</td>
<td>• Within the system itself</td>
<td>Off-line testing</td>
</tr>
<tr>
<td></td>
<td>• Applied by an external device (tester)</td>
<td>Self-testing</td>
</tr>
<tr>
<td></td>
<td>• Design errors</td>
<td>External testing</td>
</tr>
<tr>
<td>What do we test for?</td>
<td>• Fabrication errors</td>
<td>Design verification testing</td>
</tr>
<tr>
<td></td>
<td>• Fabrication defects</td>
<td>Acceptance testing</td>
</tr>
<tr>
<td></td>
<td>• Infancy physical failures</td>
<td>Burn-in</td>
</tr>
<tr>
<td></td>
<td>• Physical failures</td>
<td>Quality-assurance testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Field testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maintenance testing</td>
</tr>
<tr>
<td>Question</td>
<td>Category</td>
<td>Test Type</td>
</tr>
<tr>
<td>-------------------------------------------------------------------------</td>
<td>------------------</td>
<td>---------------------------------------</td>
</tr>
<tr>
<td>What is the physical object being tested?</td>
<td></td>
<td>Component-level testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Board-level testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>System-level testing</td>
</tr>
<tr>
<td>How are the stimuli and/or the expected response produced?</td>
<td></td>
<td>Stored-pattern testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Algorithmic testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Comparison testing</td>
</tr>
<tr>
<td>How are the stimuli applied?</td>
<td></td>
<td>Adaptive testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Types of testing (continued)

<table>
<thead>
<tr>
<th>Criterion</th>
<th>Attribute of testing method</th>
<th>Terminology</th>
</tr>
</thead>
<tbody>
<tr>
<td>How fast are the stimuli applied?</td>
<td>• Much slower than the normal operation speed</td>
<td>DC (static) testing</td>
</tr>
<tr>
<td></td>
<td>• At the normal operation speed</td>
<td>AC testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At-speed testing</td>
</tr>
<tr>
<td>What are the observed results?</td>
<td>• The entire output patterns</td>
<td>Compact testing</td>
</tr>
<tr>
<td></td>
<td>• Some function of the output patterns</td>
<td></td>
</tr>
<tr>
<td>What lines are accessible for testing?</td>
<td>• Only the I/O lines</td>
<td>Edge-pin testing</td>
</tr>
<tr>
<td></td>
<td>• I/O and internal lines</td>
<td>Guided-probe testing</td>
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<tr>
<td></td>
<td></td>
<td>Bed-of-nails testing</td>
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<td></td>
<td></td>
<td>Electron-beam testing</td>
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<td></td>
<td></td>
<td>In-circuit testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In-circuit emulation</td>
</tr>
<tr>
<td>Who checks the results?</td>
<td>• The system itself</td>
<td>Self-testing</td>
</tr>
<tr>
<td></td>
<td>• An external device (tester)</td>
<td>Self-checking</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External testing</td>
</tr>
</tbody>
</table>
Levels of modeling for a 2-bit counter

Structural model

RTL Model

Gate level model

Transistor level
**FFreak Failures**

![Graph showing failure rate vs age.](image)

- **Infant mortality phase**
- **Wear-out phase**
- **Freak Failures**

*Age (years)*

*Failure Rate*
Automatic Test Equipment Components

- Consists of:
  - Powerful computer
  - Powerful 32-bit *Digital Signal Processor* (DSP) for analog testing
  - Test Program (written in high-level language) running on the computer
  - Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)
  - *Probe Card* or *Membrane Probe* (contains electronics to measure signals on chip pin or pad)
Verification Testing

- Ferociously expensive
- May comprise:
  - Scanning Electron Microscope tests
  - Bright-Lite detection of defects
  - Electron beam testing
  - Artificial intelligence (expert system) methods
  - Repeated functional tests
Characterization Test

- Worst-case test
  - Choose test that passes/fails chips
  - Select statistically significant sample of chips
  - Repeat test for every combination of 2 or more environmental variables
  - Plot results in *Shmoo plot*
  - Diagnose and correct design errors

- Continue throughout production life of chips to improve design and process to increase yield
Shmoo Plot

$t_{OTD} (nsec.)$

* Acceptable Reading Combination
@ Unacceptable Reading Combination
Manufacturing Test

- Determines whether manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Test at speed of application or speed guaranteed by supplier
Burn-in or Stress Test

- **Process:**
  - Subject chips to high temperature & over-voltage supply, while running production tests

- **Catches:**
  - *Infant mortality* cases – these are damaged chips that will fail in the first 2 days of operation – causes bad devices to actually fail before chips are shipped to customers
  - *Freak failures* – devices having same failure mechanisms as reliable devices
A graph showing the relationship between 
failure rate and age (years).

- Infant mortality phase
- Wear-out phase
- Freak Failures
Incoming Inspection

- Can be:
  - Similar to production testing
  - More comprehensive than production testing
  - Tuned to specific systems application

- Often done for a random sample of devices
  - *Sample size* depends on device quality and system reliability requirements
  - Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost
Types of Manufacturing Tests

- *Wafer sort or probe* test – done before wafer is scribed and cut into chips
  - Includes test site characterization – specific test devices are checked with specific patterns to measure:
    - Gate threshold
    - Polysilicon field threshold
    - Poly sheet resistance, etc.
- Packaged device tests
Sub-types of Tests

- **Parametric** – measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap

- **Functional** – used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive
Two Different Meanings of Functional Test

- **ATE and Manufacturing World** – any vectors applied to cover high % of faults during manufacturing test

- **Automatic Test-Pattern Generation World** – testing with *verification vectors*, which determine whether hardware matches its specification – typically have low fault coverage (< 70 %)
Test Specifications & Plan

- **Test Specifications:**
  - Functional Characteristics
  - Type of *Device Under Test* (DUT)
  - Physical Constraints – Package, pin numbers, etc.
  - Environmental Characteristics – supply, temperature, humidity, etc.
  - Reliability – acceptance quality level (defects/million), failure rate, etc.

- **Test plan generated from specifications**
  - Type of test equipment to use
  - Types of tests
  - Fault coverage requirement
Test Data Analysis

- Uses of ATE test data:
  - Reject bad DUTS
  - Fabrication process information
  - Design weakness information

- Devices that did not fail are good only if tests covered 100% of faults

- Failure mode analysis (FMA)
  - Diagnose reasons for device failure, and find design and process weaknesses
  - Allows improvement of logic & layout design rules
Automatic Test Equipment (ATE)
ADVANTEST Model T6682 ATE
T6682 ATE Specifications

- Uses 0.35 \( \mu \text{m} \) VLSI chips in implementation
- 1024 pin channels
- Speed: 250, 500, or 1000 MHz
- Timing accuracy: +/- 200 ps
- Drive voltage: -2.5 to 6 V
- Clock/strobe accuracy: +/- 870 ps
- Clock settling resolution: 31.25 ps
- Pattern multiplexing: write 2 patterns in one ATE cycle
- Pin multiplexing: use 2 pins to control 1 DUT pin
**Pattern Generation**

- **Sequential pattern generator (SQPG):** stores 16 Mvectors of patterns to apply to DUT, vector width determined by # DUT pins
- **Algorithmic pattern generator (ALPG):** 32 independent address bits, 36 data bits
  - For memory test – has address descrambler
  - Has *address failure memory*
- **Scan pattern generator (SCPG):** supports JTAG boundary scan, greatly reduces test vector memory for full-scan testing
  - 2 Gvector or 8 Gvector sizes
Response Checking and Frame Processor

- **Response Checking:**
  - *Pulse train matching* – ATE matches patterns on 1 pin for up to 16 cycles
  - *Pattern matching mode* – matches pattern on a number of pins in 1 cycle
  - Determines whether DUT output is correct, changes patterns in real time

- **Frame Processor** – combines DUT input stimulus from pattern generators with DUT output waveform comparison

- **Strobe time** – interval after pattern application when outputs sampled
Probing

- Pin electronics (PE) – electrical buffering circuits, put as close as possible to DUT
- Uses pogo pin connector at test head
- Test head interface through custom printed circuit board to wafer prober (unpackaged chip test) or package handler (packaged chip test), touches chips through a socket (contactor)
- Uses liquid cooling
- Can independently set $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $I_{H}$, $I_{L}$, $V_{T}$ for each pin
- Parametric Measurement Unit (PMU)
Pin Electronics

Diagram:
- **DC**
- **Switch**
- **Driver**
- **Switch**
- **Programmable Load**
- **Selector**
- **Comparator**
- **VT Terminator Dynamic Clamp**
- **Switch**
- **Pin**
- **I/O Pin**
Probe Card and Probe Needles or Membrane

- **Probe card** – custom *printed circuit board* (PCB) on which DUT is mounted in socket – may contain custom measurement hardware (current test)
- **Probe needles** – come down and scratch the pads to stimulate/read pins
- **Membrane probe** – for unpackaged wafers – contacts printed on flexible membrane, pulled down onto wafer with compressed air to get wiping action
**Guided-probe testing (GPT)**

Is a technique used in board-level testing. GPT is a sequential diagnosis procedure, in which a subset of the internal accessible lines is monitored.
Bed-of-Nails Tester Concept
T6682 ATE Software

- Runs Solaris UNIX on UltraSPARC 167 MHz CPU for non-real time functions
- Runs real-time OS on UltraSPARC 200 MHz CPU for tester control
- Peripherals: disk, CD-ROM, micro-floppy, monitor, keyboard, HP GPIB, Ethernet
- *Viewpoint* software provided to debug, evaluate, & analyze VLSI chips
LTX FUSION HF ATE
Specifications

- Intended for SOC test – digital, analog, and memory test – supports scan-based test
- Modular – can be upgraded with additional instruments as test requirements change
- enVision Operating System
- 1 or 2 test heads per tester, maximum of 1024 digital pins, 1 GHz maximum test rate
- Maximum 64 M vectors memory storage
- Analog instruments: DSP-based synthesizers, digitizers, time measurement, power test, Radio Frequency (RF) source and measurement capability (4.3 GHz)
Multi-site Testing – Major Cost Reduction

- One ATE tests several (usually identical) devices at the same time
- For both probe and package test
- DUT interface board has > 1 sockets
- Add more instruments to ATE to handle multiple devices simultaneously
- Usually test 2 or 4 DUTS at a time, usually test 32 or 64 memory chips at a time
- Limits: # instruments available in ATE, type of handling equipment available for package
Electrical Parametric Testing
Typical Test Program

1. Probe test (wafer sort) – catches gross defects
2. Contact electrical test
3. Functional & layout-related test
4. DC parametric test
5. AC parametric test
   - Unacceptable voltage/current/delay at pin
   - Unacceptable device operation limits
DC Parametric Tests
Contact Test

1. Set all inputs to 0 V
2. Force current $I_{fb}$ out of pin (expect $I_{fb}$ to be 100 to 250 $\mu$A)
3. Measure pin voltage $V_{pin}$. Calculate pin resistance $R$
   - Contact short ($R = 0 \ \Omega$)
   - No problem
   - Pin open circuited ($R$ huge), $I_{fb}$ and $V_{pin}$ large
1. Set temperature to worst case, open circuit DUT outputs

2. Measure maximum device current drawn from supply $I_{CC}$ at specified voltage
   - $I_{CC} > 70$ mA (fails)
   - $40$ mA $< I_{CC} \leq 70$ mA (ok)
Output Short Current Test

1. Make chip output a 1
2. Short output pin to 0 V in PMU
3. Measure short current (but not for long, or the pin driver burns out)
   - Short current $> 40 \ \mu$A (ok)
   - Short current $\leq 40 \ \mu$A (fails)
Output Drive Current Test

1. Apply vector forcing pin to 0
2. Simultaneously force $V_{OL}$ voltage and measure $I_{OL}$
3. Repeat Step 2 for logic 1
   - $I_{OL} < 2.1 \text{ mA}$ (fails)
   - $I_{OH} < -1 \text{ mA}$ (fails)
Threshold Test

1. For each I/P pin, write logic 0 followed by propagation pattern to output. Read output. Increase input voltage in 0.1 V steps until output value is wrong

2. Repeat process, but stepping down from logic 1 by 0.1 V until output value fails
   - Wrong output when 0 input > 0.8 V (ok)
   - Wrong output when 0 input ≤ 0.8 V (fails)
   - Wrong output when 1 input < 2.0 V (ok)
   - Wrong output when 1 input ≥ 2.0 V (fails)
AC Parametric Tests
Rise/fall Time Tests

![Graph showing rise and fall times with Voltage on the y-axis and Time on the x-axis, highlighting Fall Time and Rise Time.]
Set-up and Hold Time Tests
Propagation Delay Tests

1. Apply standard output pin load (RC or RL)
2. Apply input pulse with specific rise/fall
3. Measure propagation delay from input to output
   - Delay between 5 ns and 40 ns (ok)
   - Delay outside range (fails)
Summary

- Parametric tests – determine whether pin electronics system meets digital logic voltage, current, and delay time specs
- Functional tests – determine whether internal logic/analog sub-systems behave correctly

ATE Cost Problems
- Pin inductance (expensive probing)
- Multi-GHz frequencies
- High pin count (1024)

ATE Cost Reduction
- Multi-Site Testing
- DFT methods like Built-In Self-Test
Levels of modeling for a 2-bit counter

- Structural model
- RTL Model
- Gate level model
- Transistor level