Lecture 14 – Memories

Digital Integrated Circuit Design

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Semiconductor Memory Classification

- Based on Information Storage
  - Volatile
  - Nonvolatile
- Based on Accessing to Data
  - Sequential Access Memory
  - Random Access Memory
- Based on Readable or Writeable
  - Read Only Memory (ROM)
  - Read/Write Memory (RWM)
Semiconductor Memory Classification

Conventional classification

(P)ROM
- Programmable using fusible links
- Mask programmable ROM
- EPROM
- E²PROM

RAM
- SRAM
- DRAM
### Semiconductor Memory Classification

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Memory Organization

- Such a register can be designed using D-FF for each bit
Memory Organization

- It is not economical to build large memory. Therefore memory cell circuits are simplified compare to register circuits by sacrificing most of the desired properties of digital circuits such as quantization, regeneration,…
Memory Organization

- At the level of a memory chip, the desired properties are recovered through use of properly designed peripheral circuits.
Memory Organization

- This is termed Random Access Memory (RAM)
- The name derives from the fact that memory locations (addresses) can be accessed in random order
Memory Organization

- The principal parameters
  - Read Access Time
    - Is the delay from presentation of an address until data stored at that address are available at the output
  - Cycle Time
    - Is the reciprocal of the time rate at which address information is changed while reading or writing at random location
Minimum cycle time for reading and writing are not necessarily the same. For semiconductor R/W memories, the read access time is typically 50 to 90% of read cycle time.
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ROMs

- Bipolar
- MOS
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ROMs

- Bipolar ROM and PROM Cell Arrays
  - The shortest memory access and cycle times are achieved with Bipolar transistor technology
    - Schottky ROM
    - Emitter-follower ROM
    - Emitter-follower PROM
ROMs

- Bipolar ROM and PROM Cell Arrays
  - Schottky ROM, Emitter-follower ROM
    - The schottky diode and emitter-follower ROM arrays are programmed by selectively omitting a contact at the contact mask step
ROMs

- Bipolar ROM and PROM Cell Arrays
  - Emitter-follower PROM
    - Fusible links are formed using nichrome, polysilicon, or another conductor (AL does not work) and require extra step in fabrication for deposition and patterning of this material
ROMs

- Bipolar ROM and PROM Cell Arrays
  - Emitter-follower PROM
    - The memory is programmed by selectively blowing fuse links in the desired data pattern
    - 10 to 15V voltages are necessary to force the 10 to 30 mA current to blow fuses
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ROMs

- MOS ROM Cell Arrays
  - A bit is stored in a ROM by the presence or absence of a data path from a row to a column
  - Two basic forms of MOS ROM cell arrays
ROMs

- **MOS ROM Cell Arrays**
  - In NMOS NOR array at normal operation, all but one row conductor is held low. The columns to which they are connected are pulled low. Using positive logic, a stored 1 is defined as the absence of a transistor.
ROMs

- MOS ROM Cell Arrays
  - In NAND ROM the column output goes low only when all series bit location provide a conducting path toward GND. In this case, all but one of the row are normally held at Vdd. In positive logic, a stored 1 is defined as the presence of a transistor
ROMs

- **MOS ROM Cell Arrays**
  - NOR array usually has a faster access time
  - NAND array has considerably higher bit density per unit area than NOR array
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Operation of this EPROM relies on being able to store charge on the floating gate.
EPROM and $E^2$PROM cells

- Assume no charge on the floating gate so that with gate2, drain, and source all grounded the potential of gate1 is zero. As the voltage on gate2 is increased, gate1 voltage rises also, but at a lower rate as determined by the capacitive divider $C_2-C_1$. The effect of this is to raise the threshold voltage of this transistor as seen from gate2. However, when gate2 voltage is raised sufficiently, a channel forms. Under these conditions the device provides a positive logic stored 0 when used in a NOR array.
EPROM and $E^2$PROM cells

- To write a 1, both gate2 and drain are raised to about 25V while source and substrate remain grounded
- A relatively large drain current flows
- The high field in the drain-substrate depletion region results in avalanche breakdown of the drain-substrate junction
- A small fraction of accelerated electrons traverse the thin oxide and become trapped on gate1
- When gate2 and drain potentials are reduced to zero, the negative charge on gate1 forces its potential to about -5V. If gate2 voltage for reading is limited to 5V, a channel never forms
- Thus a 1 is stored in the cell
**EPROM and E²PROM cells**

- Gate1 is completely surrounded by silicon dioxide (SiO₂), so charge can be stored for many years.
- Data may be erased by exposing the cells to ultraviolet light.
- This structure is also known as FAMOS (Floating gate Avalanche injection MOS).
EPROM and $E^2$PROM cells

- $E^2$PROM employs a somewhat different structure and a different mechanism for writing and erasing.
- A portion of the dielectric gate1 from body and drain is reduced in thickness to about 100Å.
- When about 10V is applied across this thin dielectric, electrons flow to or from gate1 by a conduction mechanism known as Fowler-Nordheim tunneling.
- This mechanism is reversible.
- For reading, operation is similar to the EPROM.
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Static R/W Memories (SRAM)

- Memories are said to be static if no periodic clock signals are required
  - Bipolar R/W Memories
  - MOS R/W Memories
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Static R/W Memories (SRAM)

- Bipolar R/W Memories
  - The first semiconductor memories employed bipolar technology
  - Bipolar memory is now used primarily where highest speed operation is required
Static R/W Memories (SRAM)

- Bipolar R/W Memories
  - Two widely used bipolar transistor cells
Bipolar R/W Memories
- EC (Emitter coupled) operation
Bipolar R/W Memories

EC operation

- Assuming a logic 1 is stored with Q1 on
- Row selection requires that both R and R* go to the positive levels
- To write a 1, C must be held low
- Collector-emitter voltage of Q1 falls quickly, removing the base drive from Q2
- When the row voltages return to standby levels, Q1 remains on with its base current coming from R2
- Cell current flows through Q1 and returns to GND through line R
- Emitter connected to C and C̅ are reverse biased in the standby condition
Static R/W Memories (SRAM)

- Bipolar R/W Memories
  - EC operation
    - To read a stored 1, the cell is selected in the same way as for writing
    - Emitters connected to R become reverse biased, and the current flowing in Q1 transfers to the emitter connected to C
    - The resulting rise in the voltage on C indicates the presence of a stored 1
  - The operations of writing and reading a 0 are complementary of those just described
Static R/W Memories (SRAM)

- Bipolar R/W Memories
  - DC (Diode coupled) operation
Static R/W Memories (SRAM)

- Bipolar R/W Memories
  - DC operation
    • Assuming a logic 1 is stored with Q2 on
    • Row selection requires that the row voltage be pulled low
    • To write a 1, the voltage on line C is raised, forward biasing diode D1
    • Sufficient current must be forced so that voltage across R3 and Q1 is adequate to turn on Q2
    • When Q2 turns on, its collector voltage drops rapidly, turning off Q1
    • In the standby condition, D1 and D2 are reverse biased
Static R/W Memories (SRAM)

- Bipolar R/W Memories
  - DC operation
    - To read a stored 1, the row is pulled low and current flows from \( \overline{C} \) through D2, R4, and Q2 to R.
    - The resulting drop in the voltage on \( C \) indicates the presence of a stored 1.
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Static R/W Memories (SRAM)

- MOS R/W Memories
Static R/W Memories (SRAM)

- MOS R/W Memories
Static R/W Memories (SRAM)

- MOS R/W Memories
  - Memory cells based on NMOS and CMOS technology

![Diagram of MOS R/W Memories]
MOS R/W Memories

- Both cells employ a pair of access devices, M3, M4, to provide a switchable path for data into and out of the cell.
- Row select line R is held low except when cells connected to it are to be accessed for reading or writing.
- Two column lines, C and \( \overline{C} \), provide the data path.
- In principal, it should be possible to achieve all memory functions using only one column line and one access device. But due to normal variations in device parameters and operating conditions, it is difficult to obtain reliable operation at full speed using a single access line.
- Therefore, the symmetrical data path C and \( \overline{C} \) are almost always used.
MOS R/W Memories

Operation of both cells proceeds as follows

- The row selection line, held low in the standby state, goes to Vdd
- Turning on access transistors M3 and M4
- Writing is accomplished by forcing either C or \( \overline{C} \) low, while the other remains at about 3V
Static R/W Memories (SRAM)

- MOS R/W Memories
  - To write a 1
    - $\overline{C}$ is forced low
      - The cell must be designed such that the conductance of M4 is several times larger than that of M6 so that the drain of M2 and gate of M1 may be brought below VT
    - M1 turns off and its drain voltage rises due to the currents from M5 and M3
    - M2 turns on and the row line may return to its low standby level, leaving the cell in the desired state
Static R/W Memories (SRAM)

- MOS R/W Memories
  - To read a 1
    - C and C are initially biased at about 3V
    - When the cell is selected, current flows through M4 and M2 to GND and through M5 and M3 to C
    - The gate voltage of M2 does not fall below 3V, so it remains on
      - To avoid altering the state of the cell when reading, then conductance of M2 must be about 3 times that of M4 so that the drain voltage of M2 does not rise about VT
Static R/W Memories (SRAM)

- MOS R/W Memories
  - The operations of writing and reading a 0 are complementary to those just described
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Problems with SRAM

- Six transistors use up lots of area
- Consider a “Zero” is stored in the cell
  - Transistor N1 will try to pull “bit” to 0
  - Transistor P2 will try to pull “bit bar” to 1
- If Bit lines are pre-charged high: are P1 and P2 really necessary?
  - Read starts by precharging bit and ~bit
  - Selected cell pulls one of them low
  - Sense the difference
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Static R/W Memories (SRAM)

- 6-transistor CMOS SRAM Cell Layout
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Dynamic R/W Memories

- The static memory cells described so far all require four to six transistors per cell and four or five lines connecting to each cell.
- In the late 1960s it was realized that memory cells with reduced complexity, area, and power consumption could be designed if dynamic MOS circuits concepts were used.
- Dynamic cells store binary data as charge on a capacitance.
- Normal leakage currents can remove stored charge in a few ms, so dynamic memories require periodic restoration, or refreshing, of stored charge, typically every 2 or 4 ms.
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Dynamic R/W Memories

- **3-Transistor DRAM Cell**
  - The first widely used dynamic memory cell
Dynamic R/W Memories

3-Transistor DRAM Cell

- Precharge \( \Phi_1 \)
- RS(\( \Phi_2 \))
- WS(\( \Phi_2 \))

\[ \text{Write1, Read1, Write0, Read0} \]
3-Transistor DRAM Cell

- Does not require internal device conductance ratio for proper operation
- M2, M3, and M4 can all be small devices to minimize cell area
- C1 is parasitic node capacitance and it is essential to normal operation
- Charge stored on C1 represents stored binary data
- Selection lines for reading and writing must be separated because the stored charge on C1 would be lost if M3 turned on during reading
- Column lines for data in (D_{in}) and data out (D_{out}), may be combined at the expense of some extra complexity in the read-write circuits
Dynamic R/W Memories

- **3-Transistor DRAM Cell**
  - The cell operates in two-phase cycles
  - The first half of each read or write cycle is devoted to a precharge phase during which columns $D_{in}$ and $D_{out}$ are charged to a valid high logic level via $M_{Y1}$ and $M_{Y2}$
  - The $D_{in}$ line is highly capacitive because it joins many cells
  - The read-write circuits do not need to hold $D_{in}$ high because sharing the charge on $D_{in}$ with $C1$ does not significantly reduce the precharge high level
  - A 0 is written by turning on $M3$ after the precharge phase is over, then simultaneously discharge $D_{in}$ and $C1$ via a grounded-source pull-down device (not shown) in the R/W circuit
  - Reading is accomplished by turning on $M4$ after the precharge is over
  - If a 1 is stored, $D_{out}$ will be discharged through $M2$ and $M4$
  - If a 0 is stored, there will be no conducting path through $M2$, so the precharge high level on $D_{out}$ will not change
Dynamic R/W Memories

- **3-Transistor DRAM Cell**
  - The cell may be read repeatedly without disturbing the charge stored on C1.
  - The drain junction leakage of M3 depletes the stored charge over the span of many milliseconds.
  - Refreshing is performed by reading stored data before they all leak away, inverting the result, and writing back into the same location. This is done simultaneously for all the bits in a row once every 2 or 4 ms.
  - The level on the D\textsubscript{out} line in principle can be detected with a simple inverter.
  - If a short access time is desired, a sense circuit would be used.
  - Use of the dynamic precharge reduces power consumption compared to static NMOS operation.
  - If the D\textsubscript{out} high level were to be established only through a static pull-up device, higher average current drain would be required for D\textsubscript{out} to recover a high level after reading a 1.
Dynamic R/W Memories

- **3-Transistor DRAM Cell**
  - Similarly, fast changes of state on $D_{in}$ would require excessive power if static drivers were used.
  - For this 3T cell, output data are inverted compared to input data. However, memory component data input and output will have the same logic polarity if one extra inversion is included in either the read or write data path.
Dynamic R/W Memories

- 3-Transistor DRAM Cell
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Dynamic R/W Memories

- **1-Transistor DRAM Cell**
  - Most modern dynamic RAMs use 1T cell

![Diagram of 1-Transistor DRAM Cell]
Dynamic R/W Memories

1-Transistor DRAM Cell

- Selection for reading or writing is accomplished by turning on M1 with the single row line.
- Data are stored as a high or low level on C1.
- In the interest of minimum cell area, C1 is very small, on the order of 30 to 100 fF.
- The selection signal on the row line is the same for reading or writing.
- Data are written into the cell by forcing a high or low level on the column when the cell is selected.
Dynamic R/W Memories

1-Transistor DRAM Cell

- When reading, the charge stored on C1 is shared with the 10 to 20 times larger capacitance C2 of the column line.
- Considering that after 2ms the difference in stored voltage between a 1 and a 0 may be as little as 2V, the data output signal may be as small as 100mV.
- Stored data must be regenerated every time they are read, in addition to refreshing them every 2ms even if they are not read.
- Read amplifier design for reliable detection of the small column is one of the most difficult aspect of 1T dynamic RAM design.
1-Transistor DRAM Cell

- **Write**
  - Drive bit line
  - Select row

- **Read**
  - Precharge bit line to Vdd/2
  - Select row
  - Cell and bit line share charges
    - Minute voltage changes on the bit line
  - Sense (fancy sense amp)
    - Can detect changes of ~1 million electrons
  - Write: restore the value

- **Refresh**
  - Just do a dummy read to every cell
1-Transistor DRAM Cell

Reading

- To read the bit stored in the cell, the cell is connected to a floating bit line.
- Notice that the bit line has its own parasitic capacitance $C_b$, that is usually much larger than $C$.
- When the connection is established, the charge $Q$ stored in the cell (c) redistributes between $C$ and $C_b$.
- If $C_b$ was originally empty, and the value stored in the cell was 1, the result of the charge redistribution process is a voltage level that is below the logic threshold $V_{dd}/2$, and is not recognized as a logic 1.
Dynamic R/W Memories

1-Transistor DRAM Cell

Reading

- To solve this problem, the bit line needs to be pre-charged at Vdd/2, so that the redistribution of the charge stored in the cell causes the final voltage level to be above or below Vdd/2, according to the value of the stored bit.
Dynamic R/W Memories

- **1-Transistor DRAM Cell**
  - **Writing**
    - To write a bit (say b) in the cell, the bit line BL is driven to the target value of b while asserting WL
    - When the capacitor is connected to a driven line, it is charged or discharged in order to reach the voltage level of the driven line
    - The connection of a capacitor C to power supply (ground) can be viewed as the connection of a section-C reservoir to a second reservoir with infinite section filled of fluid up to level Vdd (or 0)
1-Transistor DRAM Cell

The simplified schematic for a read-refresh circuit for a 1T RAM
1-Transistor DRAM Cell

- The regenerative switching of a dynamic FF detects the small signal and restores the high or low signal level. The storage array is split in half so that equal capacitances are connected to each side of the FF.
1-Transistor DRAM Cell

Sequence of signals for reading

- A precharge clock phase $\Phi_p$ sets the voltage on all column lines near the supply level $V_{dd}$ and sets the voltage in all dummy cells to zero.
- One row (either in the left or right array of storage cells) is then selected with a signal $\Phi_R$.
- The dummy cell on the opposite side of the sense amplifier is selected simultaneously with a signal $\Phi_D$.
- The column voltage on the side connected to the selected dummy cell drops slightly as the column charge is shared with the dummy cell capacitance.
- The column voltage on the side connected to the selected storage cell drops twice as much (if a 0 was stored) or does not change (if a 1 was stored).
- The resulting small voltage difference between the two sides of the array determines the final state of the FF when latching signal $\Phi_S$ is applied.
- Note that if no dummy cell were used here, there would be no voltage difference between the two sides for a stored 1.
Dynamic R/W Memories

1-Transistor DRAM Cell

- Circuit noise or unbalance then would determine the latched result
- The data are taken out through a column decoder circuit to a final amplifier and output buffer
- The timing diagram shows the sequence of signals that appear when a stored 0 level is read from the left half of the array
Dynamic R/W Memories

- **1-Transistor DRAM Cell**
  - Observations
    - 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
    - DRAM memory cells are single ended in contrast to SRAM cells
    - The read-out of the 1T DRAM cell is destructive
    - Read and refresh operations are necessary for correct operation
    - Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design
    - When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than Vdd
Dynamic R/W Memories

- 1-Transistor DRAM Cell

Cross-section

Uses Polysilicon-Diffusion Capacitance
Expensive in Area

Layout
Contents

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  - MOS ROM Cell Arrays
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- **Static R/W Memories (SRAM)**
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- **Dynamic R/W Memories**
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  - 1-Transistor DRAM Cell
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  - More recent DRAM enhancements
  - Periphery
  - DRAM Architecture
  - Giga-bit DRAM
- **Summary**
Dynamic R/W Memories

- **DRAM Storage Capacitor**
  - **Planar Capacitor**
    - Up to 1Mb
    - C decreases linearly with feature size
  - **Trench Capacitor**
    - 4–256 Mb
    - Lining of hole in substrate
  - **Stacked Cell**
    - > 1Gb
    - On top of substrate
    - Use high $\varepsilon$ dielectric

\[ C = \varepsilon A/d \]
Dynamic R/W Memories

- DRAM Storage Capacitor
  - Trench Capacitor
    - Process
      - Etch deep hole in substrate
        » Becomes reference plate
      - Grow oxide on walls
        » Dielectric
      - Fill with polysilicon plug
        » Tied to storage node

- SiO₂ Dielectric
- Storage Plate
- Reference Plate
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Dynamic R/W Memories

- More recent DRAM enhancements
  - EDO - extended data out (similar to fast-page mode)
    - RAS cycle fetched rows of data from cell array blocks (long access time, around 100ns)
    - Subsequent CAS cycles quickly access data from row buffers if within an address page (page is around 256 Bytes)
  - SDRAM - synchronous DRAM
    - clocked interface
    - uses dual banks internally. Start access in one bank then next, then receive data from first then second
  - DDR - Double data rate SDRAM
    - Uses both rising (positive edge) and falling (negative) edge of clock for data transfer. (typical 100MHz clock with 200 MHz transfer)
  - RDRAM - Rambus DRAM
    - Entire data blocks are access and transferred out on a high-speed bus-like interface (500 MB/s, 1.6 GB/s)
    - Tricky system level design. More expensive memory chips
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Dynamic R/W Memories

- Periphery
  - Decoders
  - Sense Amplifiers
  - Input/Output Buffers
  - Control/Timing Circuit
Dynamic R/W Memories

- Periphery
  - Sense Amplifiers

\[ t_p = C \frac{\Delta V}{I_{av}} \]

- C large
- \( I_{av} \) small
- \( t_p \) small
Dynamic R/W Memories

- Periphery
  - Sense Amplifiers
    - single ended current mirror amplifier
Dynamic R/W Memories

- Periphery
  - Sense Amplifiers
    - Double ended current mirror amplifier
Dynamic R/W Memories

- Periphery
  - Sense Amplifiers
    - Cross coupled amplifier

![Diagram of a cross coupled amplifier](image-url)
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Dynamic R/W Memories

- DRAM Architecture

Writing a bit=1 at Word 0, bit position 5
Dynamic R/W Memories

- DRAM Architecture
  - Open Bitline Architecture
Dynamic R/W Memories

- DRAM Architecture
  - Open Bitline Architecture
Dynamic R/W Memories

- DRAM Architecture
  - Folded-Bitline Architecture
Dynamic R/W Memories

- DRAM Architecture
  - Transposed-Bitline Architecture

(a) Straightforward bitline routing.

(b) Transposed bitline architecture.
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Dynamic R/W Memories

- Giga-bit DRAM
  - One 4 Giga DRAM stores the complete work of Shakespeare 64 times!
  - 64 Gbit DRAM expected in 2016!
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Summary

- This lecture begins by defining special terms used in the description of semiconductor memories. Analysis and design of static and dynamic RAM are fully described. It is shown that elements such as sense amplifier which is one of the important periphery of any dynamic RAM, require careful circuit design.