Digital Integrated Circuit Design

Lecture 11 – BiCMOS

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Contents

- Introduction
- BiCMOS Devices
- BiCMOS Inverters
- BiCMOS Gates
- BiCMOS Drivers
- How to Choose a Logic Style
- Designing Fast CMOS Gates
- Summary
Introduction

- BiCMOS is a logic family that combines Bipolar and CMOS devices into single integrated circuits
  - Higher speed
  - Lower power dissipation
  - Higher packing densities
Introduction

- Note that CMOS has an advantage over bipolar in the areas of lower power dissipation, larger noise margins, and greater packing densities, while bipolar has advantages over CMOS in faster switching speed and larger current capability.
Introduction

- BiCMOS
  - Advantages:
    - Lower power dissipation than bipolar
    - Improved speed in comparison to CMOS
    - Larger current drive than CMOS
  
  - Disadvantages:
    - Higher cost
    - Larger fabrication time (more mask steps)
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BiCMOS Devices

- Active Devices:
  - NMOS
  - PMOS
  - NPN BJT
  - Lateral PNP BJT (Vertical PNPs are less used)

- Note: CMOS process uses a double polysilicon technique, while the BJT process requires polysilicon emitters!
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BiCMOS Inverters

- Resistive Shunts
  - Has full logic swing (0 to Vdd) by the passive resistors R1, R2. However, since uses resistors, it is not practical
  - $V_{OH} = Vdd$ (by R1, M1)
  - $V_{OL} = 0$ (by R1, M2, R2)
BiCMOS Inverters

- Active Shunts
  - Each BJTs have a MOSFET in parallel and does not provide full rail-to-rail swing
  - $V_{OH} = V_{dd} - V_{BEon(1)}$
  - $V_{OL} = V_{BEon(2)}$
BiCMOS Inverters

- **R-Type BiCMOS**
  - R1 and R2 form the bleeding path and provide full rail-to-rail swing
  - $V_{OH} = V_{dd}$
  - $V_{OL} = 0$

- **Disadvantages**
  - Current ratio in BJT is reduced
BiCMOS Inverters

- R-Type (Active) BiCMOS
  - M3 and M4 must be chosen to be in triode region
BiCMOS Inverters

- Feedback Type BiCMOS
  - Inverter forms a Positive Feedback
  - It removes the low current ratio in BJT

![BiCMOS Inverter Circuit Diagram]
BiCMOS Inverters

- With parallel output CMOS (Collector-Emitter Shunting)
  - Logic swing can be increased to the full power supply voltage by adding pull-up and pull-down shunt resistors (active transistors) between the collector and emitter of each BJT
- Full rail-to-rail swing
- $V_{OH} = V_{dd}$ (By M5)
- $V_{OL} = 0$ (By M6)
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BiCMOS Gates

- General Structure

![BiCMOS Gate Diagram](image)

- PMOS Array
- NMOS Array
- Q1
- Q2
- Y
BiCMOS Gates

- NAND (Resistive Shunt)
  - The basic operation of this gate is described by considering the MOSFETs first, realizing that the BJTs perform as output buffers.
BiCMOS Gates

- NAND (Active Shunt)
BiCMOS Gates

- Merged Bipolar-CMOS Current Mode
  - NMOS is On or Off depend on level of the input
- Advantages
  - As ECL gate, the Vdd current is constant in all of states
BiCMOS Gates

- Merged Bipolar-CMOS Current Mode
  - It is possible to have Current Spikes
  - If B =1, A = C =0 and then A =1 we have current spike

![BiCMOS Circuit Diagram]
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BiCMOS Drivers

- BJT s are used to drive output nodes
- There are four types of drivers
  - Common Collector NPN-PNP
  - Gated Diode
  - Emitter Follower
  - Modified Gated Diode
- In each circuit, MOSFETs are used as switches to supply base current to the BJT s
BiCMOS Drivers

- Common Collector NPN-PNP (Collectors are in Common)
  - $A = 0$, NMOS is off and PMOS is on
  - NPN to be cutoff and PNP to be in saturation
  - $V_{out} = V_{dd} - V_{ECSat} = V_{OH}$
  - $A = V_{dd}$, NMOS turns on and PMOS turns off
  - PNP = Off, NPN = Sat.
  - $V_{out} = V_{CESat} = V_{OL}$
BiCMOS Drivers

- Common Collector NPN-PNP
  - Swing is less than rail-to-rail
  - PNP and NPN saturate, the switching speed from output low to high is reduced
  - If PNP and NPN are replaced with schottky BJTs, this switching time is improved
  - Static power dissipation is also exist
BiCMOS Drivers

- Gated Diode
  - It is an improved driver
  - Each MOSFET acts as a switch between the base and collector of the BJTs. When the switch is on, the corresponding BJT becomes a diode

\[
\begin{align*}
V_{in} = 0 & \Rightarrow M1 = \text{off}, \ M2 = \text{on}, \ Q2 = \text{active}, \ V_{out} = Vdd - V_{EBon} \\
V_{in} = Vdd & \Rightarrow M1 = \text{on}, \ M2 = \text{off}, \ Q1 = \text{active}, \ V_{out} = V_{BEon}
\end{align*}
\]
BiCMOS Drivers

- **Modified Gated Diode**
  - This circuit has two additional NMOS transistors (M2, M3) that provide a discharge path for the base current of the output BJTs
  - M2 discharges Q2 when output High
  - M3 discharges Q1 when output Low
- **Note:** Output is inverted of Input
BiCMOS Drivers

- Emitter Follower
  - Each MOSFET operates as an inverter

\[
V_{OH} = V_{dd} - V_{BEon} \\
V_{OL} = V_{EBon}
\]
BiCMOS Drivers

- Emitter Follower
  - Has no body effect (why=?)
  - Each MOSFET-BJT pair can be merged into a compact structure that uses less chip area (using common region for the base of the BJT and drain of the MOSFET)
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How to Choose a Logic Style

- Static CMOS
  - Easy to design
  - Robust in presence of noise
  - More amenable to voltage scaling
  - Expensive in terms of performance and area

- Pseudo-NMOS
  - Simple and fast
  - Reduced noise margin
  - Static power dissipation
How to Choose a Logic Style

- Dynamic logic
  - Potentially fast and compact
  - Difficult to design (monotonicity, leakage, noise, clocking, etc.)
- Pass Transistor Logic
  - Attractive for some specific circuits
    - e.g., MUX, XOR-dominated logic like adders
How to Choose a Logic Style

- Comparison of Logic Families

<table>
<thead>
<tr>
<th>Table 6.4</th>
<th>Comparison of circuit families</th>
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<tbody>
<tr>
<td>Family</td>
<td>nMOS</td>
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<tr>
<td>Static CMOS</td>
<td>k</td>
</tr>
<tr>
<td>Pseudo-nMOS</td>
<td>k</td>
</tr>
<tr>
<td>SFPL</td>
<td>2k+2</td>
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<tr>
<td>CVSL</td>
<td>2k</td>
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<tr>
<td>Dynamic</td>
<td>k+1</td>
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<tr>
<td>Domino</td>
<td>k+2</td>
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<td>Dual-rail Domino</td>
<td>2k+3</td>
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<td>LEAP</td>
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<td>2k+7</td>
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<tr>
<td>BiCMOS</td>
<td>2k+1</td>
</tr>
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Designing Fast CMOS Gates

- Transistor sizing
- Progressive transistor sizing
  - MOSFET closest to the output is smallest of series MOSFETs
- Transistor ordering
  - put latest arriving signal closest to the output
- Logic structure reordering
  - replace large fan-in gates with smaller fan-in gate network
- Apply “logical effort”
- Buffer (inverter) insertion
  - separate large fan-in from large $C_L$ with buffers
  - uses buffers so there are no more than four TGs in series
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Summary

- This lecture describes the basic BiCMOS Logic Gates, Inverters, Drivers and also implementation of them in transistor level
- Also noted how to choose a logic style and designing fast CMOS gates